

BOOST ISO120 BANDWIDTH TO MORE THAN 100kHz

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There has been considerable demand for high-bandwidth isolation amplifiers. The highest bandwidth Burr-Brown ISO amps are the ISO100 and the ISO120/121/122 family with bandwidths of about 50kHz. The ISO120/121 bandwidth can be boosted to more than 100kHz by adding gain in the feedback.

Adding gain in the feedback of the ISO120/121 increases bandwidth and decreases phase margin—see Figure 4. The ISO120 was designed with approximately 70° phase margin in the output stage for maximally flat magnitude response and a f_{-3dB} bandwidth of approximately 50kHz. With a gain of 2.4V/V in the feedback as shown in Figure 1, phase margin is decreased to an acceptable 45°. Due to gain peaking, the actual f_{-3dB} bandwidth is increased to almost 150kHz. With the addition of an input filter as shown in Figure 2, flat magnitude response with a bandwidth of

greater than 100kHz is obtained. Since the added gain is within the ISO120 feedback loop, the overall gain of the isolation amplifier is unchanged (gain = 1).

To verify the phase margin, analyze the step response of the Figure 1 circuit (shown in the Scope Photo 1). The 25% overshoot translates to a damping factor of 0.4 and 45° phase margin.

If the ISO120 is used in the clocked mode, maximum bandwidth is determined by the clock frequency. For 150kHz bandwidth and 45° phase margin with a gain of 2.4V/V in the ISO120 feedback, the clock frequency should be 500kHz. Lower clock frequencies will result in reduced phase margin and possible instability. Higher clock frequencies will result in better phase margin, but clock frequencies above 700kHz are not recommended.

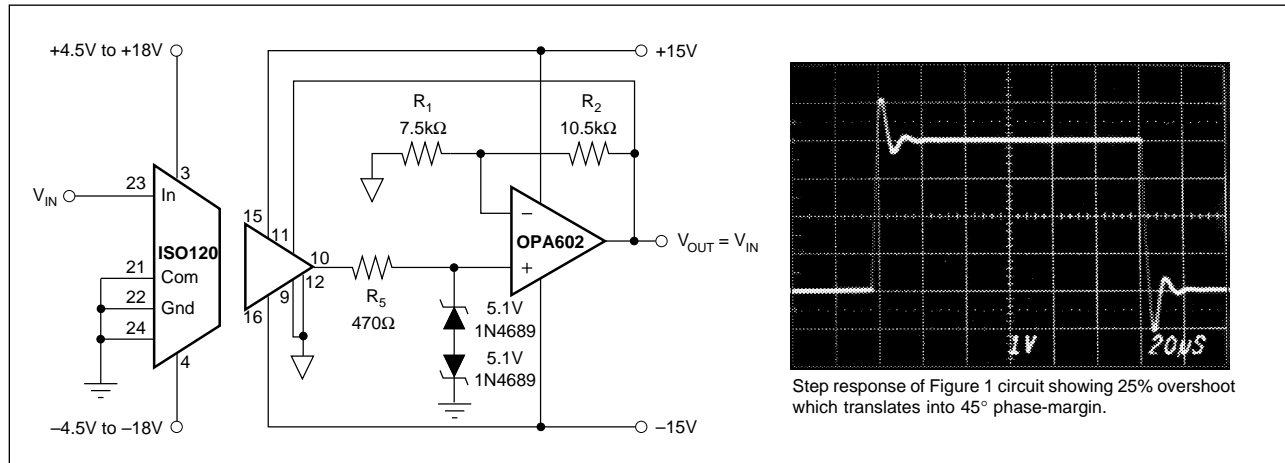


FIGURE 1. ISO120 with f_{-3dB} Bandwidth Boosted to Approximately 150kHz.

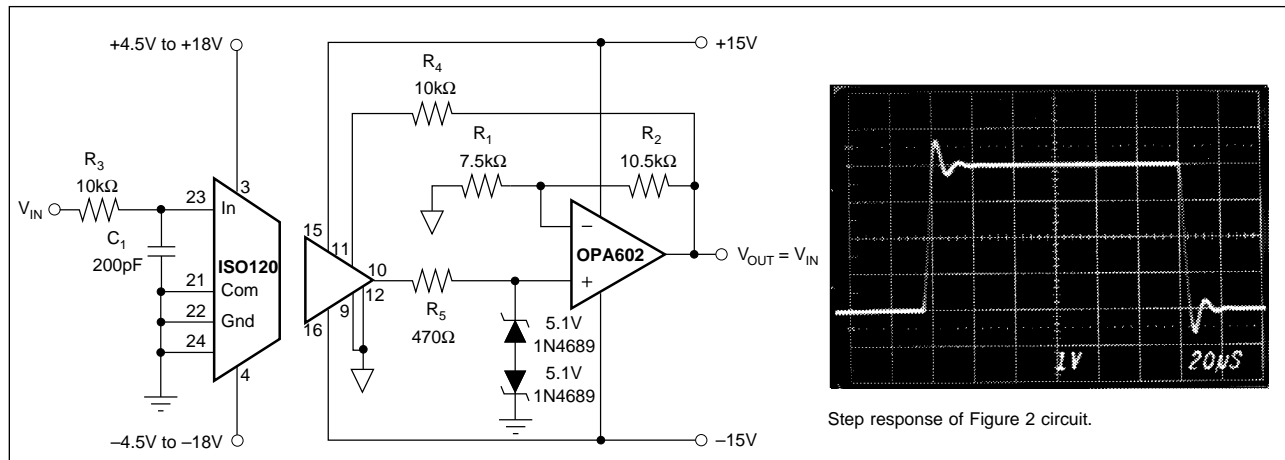


FIGURE 2. ISO120 with Flat Magnitude Response and f_{-3dB} Bandwidth Boosted to More Than 100kHz.

Adding gain in the feedback of the ISO120 can also increase its slew rate and full-power response. So long as the op amp providing gain in the feedback has adequate slew rate, the 2V/ μ s slew rate of the ISO120 is multiplied by its gain. When using an OPA602 with a gain of 2.4V/V in the feedback, the 30kHz 20Vp-p full-power response of the ISO120 is increased to more than 70kHz. Driving the OPA602 input below about -12V will cause signal inversion and possible circuit lock-up. The 470 Ω /back-to-back zener network prevents possible lock-up by keeping the op amp input from being driven beyond its linear common-mode input range.

The addition of an input filter to compensate for the gain peaking, as shown in Figure 2, gives a flat magnitude response of more than 100kHz. In addition to the gain of

2.4V/V amplifier in the feedback, a simple 80kHz input filter formed by C_1 and R_3 is inserted at the input. The 10k Ω input resistor, R_3 , decreases the ISO120 gain by about 5%. A matching 10k Ω resistor in the feedback, R_4 , restores gain accuracy. The step response for the Figure 2 circuit is shown in the scope photo.

The Gain vs Frequency Plot, Figure 3, compares the response of the Figure 1 and Figure 2 circuits, to the standard ISO120. The top plot is the Figure 1 circuit showing about +3dB magnitude peaking and almost 150kHz f_{-3dB} bandwidth. The center plot is the Figure 2 circuit with the 80kHz input filter. The magnitude response is flat with an f_{-3dB} bandwidth greater than 100kHz. The bottom plot shows the standard ISO120 circuit with an f_{-3dB} bandwidth of about 50kHz.

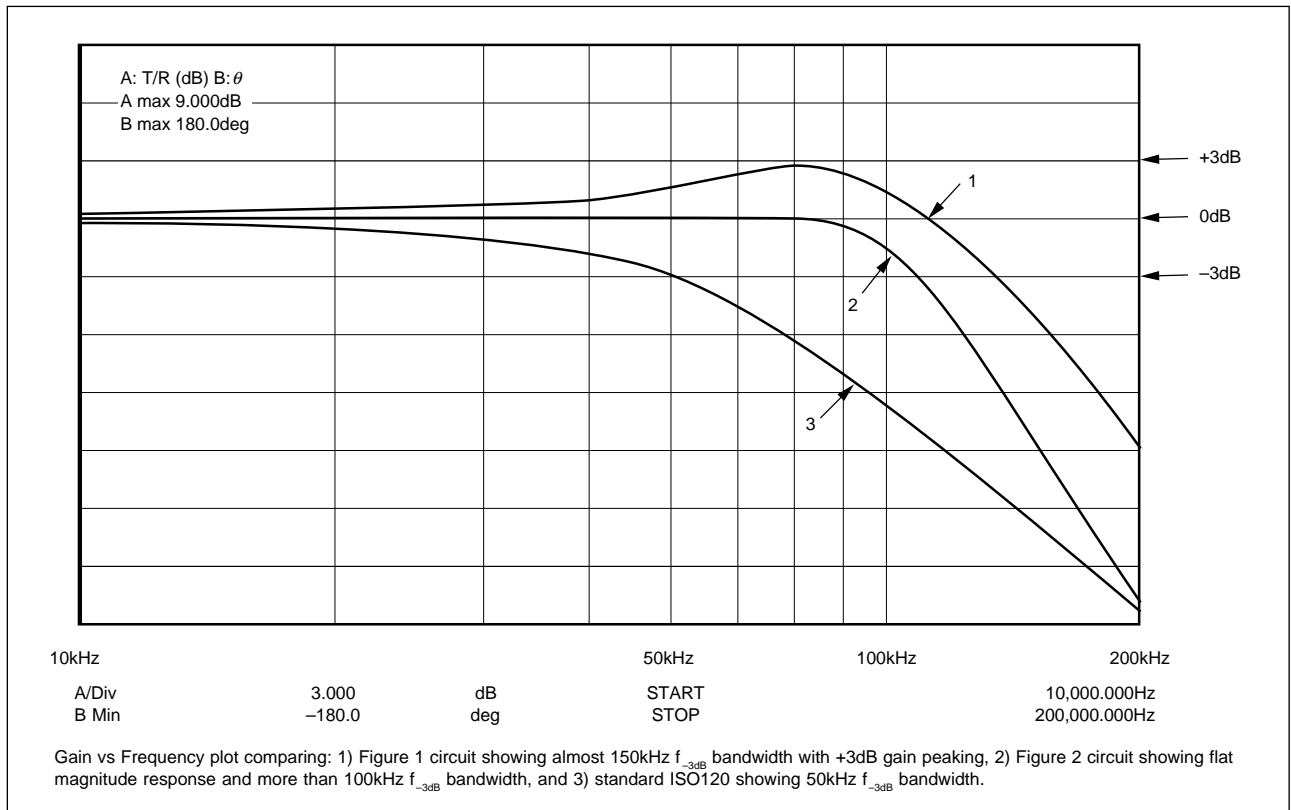
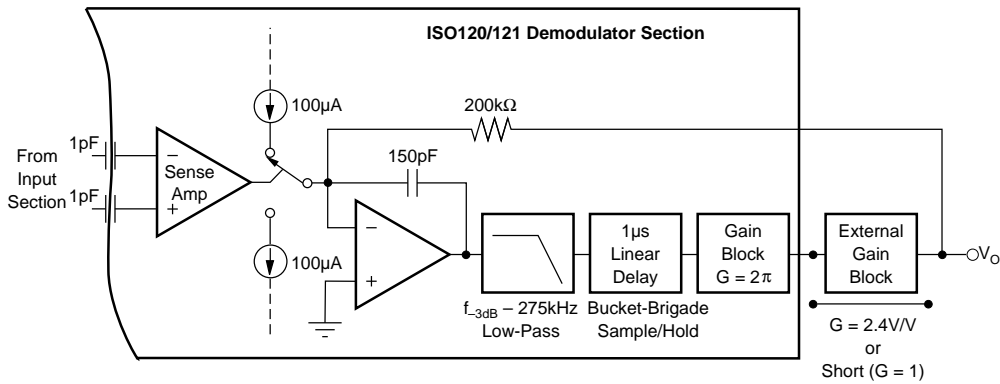


FIGURE 3. Gain vs Frequency Plot.



The output demodulator section of the ISO120/121/122 consists of the integrator loop shown. This technique can not be applied to the ISO122 because the feedback connection is not available externally. Stability is determined by the phase margin at the open-loop response unity gain point, f_{UG} .

The unity-gain frequency is:

$$f_{UG} = \frac{6.28 \cdot \text{gain}_{EXT}}{2 \cdot \pi (200k\Omega) \cdot (150pF)} = 33kHz \cdot \text{gain}_{EXT}$$

The phase margin is approximated by:

$$180^\circ - \underbrace{90^\circ}_{200k\Omega, 150pF \text{ integrator}} - \underbrace{\tan^{-1}(f_{UG}/275kHz)}_{\text{higher order poles}} - \underbrace{1\mu s \cdot f_{UG} \cdot 360^\circ}_{\text{sample/hold delay}^*}$$

*The sample/hold delay is $1/(2 \cdot \text{freq}_{CLK})$. For a 500kHz clock frequency, the delay is 1µs. The free-running clock frequency is approximately 500kHz.

For $\text{gain}_{EXT} = 1$:

$f_{UG} = 33kHz$, Phase Margin = 70°, and

$f_{-3dB} = 50kHz$

For $\text{gain}_{EXT} = 2.4$:

$f_{UG} = 80kHz$, phase margin = 45°, and

$f_{-3dB} = 150kHz$ with +3dB gain peaking at 80kHz.

FIGURE 4. Analysis of ISO120/121 Demodulator Section.

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